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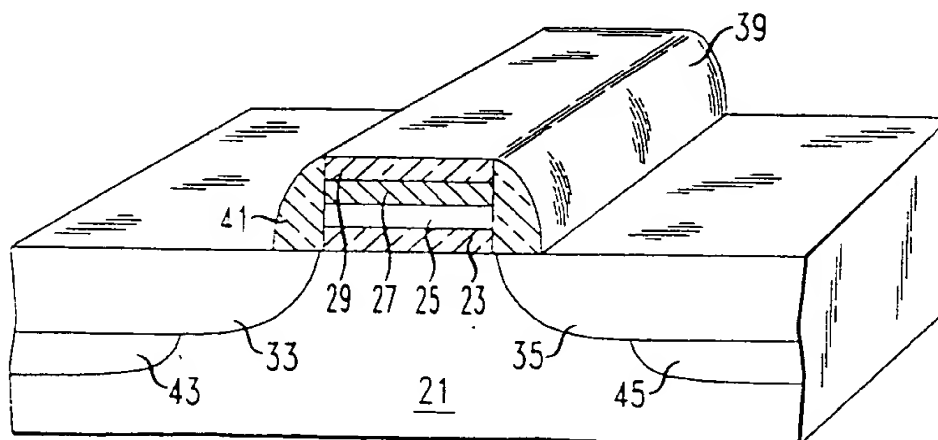
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## (54) Dual gate formation

(57) A structure and method for fabrication of an integrated circuit having adjoining  $n^+$  and  $p^+$  gates (25, 31) is disclosed. The adjoining  $n^+$  and  $p^+$  gates are covered by a titanium nitride layer (27). The titanium nitride layer is covered by a protective layer (29) illustratively made from PETEOS and by flanking spacers (not shown in

FIG. 2). The protective layers help to prevent oxidation of the titanium nitride layer. (Oxidation of the titanium nitride layer would destroy its shunting capability.) Also disclosed is a heating step which simultaneously activates source/drain implants as well as flowing an overlying dielectric

FIG. 4



## Description

### Technical Field

This invention relates to semiconductor integrated circuits and their manufacture

### Background of the Invention

Those who manufacture MOS integrated circuits are utilizing designs in which both  $n^+$  and  $p^+$  gates are contained within the same integrated circuit

Unfortunately, when an  $n^+$  gate contacts a  $p^+$  gate counterdoping may occur and a region of poor conductivity may occur where the  $n^+$  and the  $p^+$  gate contact each other

An attempt at solving the problem is depicted in FIG. 1. In FIG. 1, reference numeral 11 denotes a substrate which may typically be silicon. Reference numeral 13 denotes a gate, made from patterned,  $n^+$  doped polysilicon. Reference numeral 15 denotes a  $p^+$  doped patterned polysilicon. Typically, gates 13 and 15 are patterned together from the same blanket layer of polysilicon, although each has been doped separately while the other has been masked. There is an opportunity for counterdoping at boundary 19 between gates 13 and 15. Layer 17 is made from titanium nitride. Titanium nitride layer 17 acts as a shunt over gates 13 and 15 and preserves conductivity across boundary 19 where an  $n^+$ - $p^+$  diode exists. Unfortunately, titanium nitride layer 17 is easily oxidized, and its conductivity thereby substantially reduced if thermal processing temperatures go to 800°C or above.

Those concerned with the development of integrated circuits have consistently sought for methods to preserve conductivity across the  $n^+$ / $p^+$  gate boundary despite the problems posed by subsequent thermal processing. Furthermore, those concerned with the development of integrated circuits have continually sought methods of reducing thermal budgets.

### Summary of the Invention

The present invention as set out in the independent claims addresses the above concerns. Illustratively, the invention includes a substrate with a gate structure having a patterned dielectric layer. The dielectric layer has first and second portions. A layer of patterned  $n$  doped polysilicon is over the first portion of the dielectric. A layer of patterned  $p$  doped polysilicon is over the second portion of the dielectric. A patterned layer of conductive material is over the  $n$  doped polysilicon and the  $p$  doped polysilicon. A patterned dielectric layer is over the layer of conductive material; the dielectric layer does not contact the substrate. The gate also has sides and has spacers contacting the sides, whereby the conductive layer is enclosed by: a) the patterned dielectric layer; b) the spacers; c) the  $n$  doped polysilicon and d) the  $p$

doped silicon.

In another embodiment, the invention includes a method of forming an integrated circuit by forming adjacent  $n$  and  $p$  doped gates over a substrate. A conductive shunt layer is formed over the gates. The conductive shunt layer has a top and sides. A patterned dielectric layer is formed which covers the top of the conductive shunt layer and does not cover the substrate. Then spacers are formed which contact the sides of the conductive shunt layer.

A further embodiment of the present invention is a method of integrated circuit fabrication which includes forming source and drain regions in a substrate by implanting dopants. Then a dielectric is formed over the source and drain regions. Then a heating step is performed which simultaneously activates the dopants and smooths the dielectric by causing the dielectric to flow. Then a window is opened through the dielectric thereby exposing the source or drain region.

### Brief Description of the Drawings

FIG. 1 is a cross-sectional view of the typical prior art device.

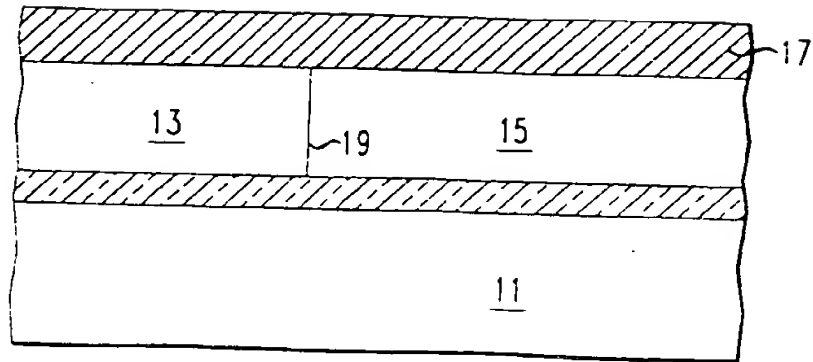
FIGS. 2-5 are partially cross-sectional, partially perspective drawings showing an illustrative embodiment of the present invention.

### Detailed Description

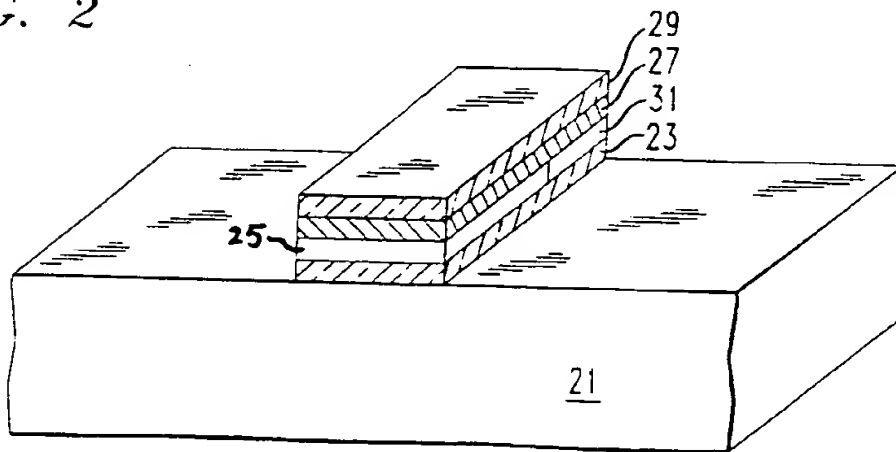
In FIG. 2, reference numeral 21 denotes a substrate which, typically, may be silicon, doped silicon, epitaxial silicon, etc. In general, the term "substrate" is used to refer to a body of material upon which other bodies or layers of material may be subsequently formed. Formed atop substrate 21 is gate oxide layer 23.  $n^+$  polysilicon gate layer 25 is formed atop gate oxide 23.  $p^+$  doped polysilicon gate 31 is also formed atop gate oxide 23.  $p^+$  gate 31 contacts  $n^+$  gate 25. Titanium nitride layer 27 is located on top of gate 25 and 31. Titanium nitride layer 27 contacts both gates 25 and 31 and electrically shunts them. Layer 29 is a dielectric, desirably formed from plasma enhanced tetraethoxysilane (PETEOS). Applicant has determined that dielectrics formed from low pressure CVD TEOS are unsatisfactory because the dielectric deposition process causes undue oxidation of titanium nitride layer 25 during deposition. Silicon nitride has also been found to be unsuitable for layer 29 because subsequent etching of the silicon nitride/polysilicon/oxide stack is very difficult. Other acceptable dielectrics for layer 29 may be spin on glass (SOG) or Low Temperature Oxides (desirably formed below 400°C).

The process for creating the structure of FIG. 2 may, typically, involve depositing a blanket layer of oxide over substrate 21. Next, a blanket layer of polysilicon is deposited over the oxide layer. The polysilicon is then doped utilizing  $p^+$  and  $n^+$  dopants in the appropriate places. Next, blanket layers of titanium nitride and PE-

*FIG. 1*  
(PRIOR ART)



*FIG. 2*



*FIG. 3*

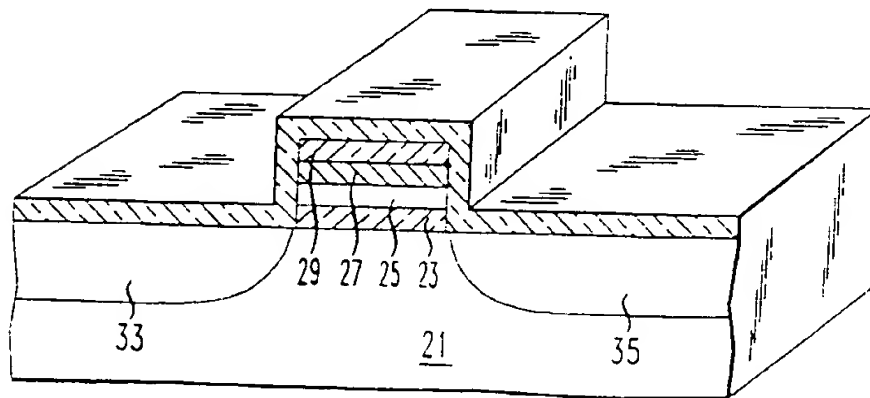


FIG. 4

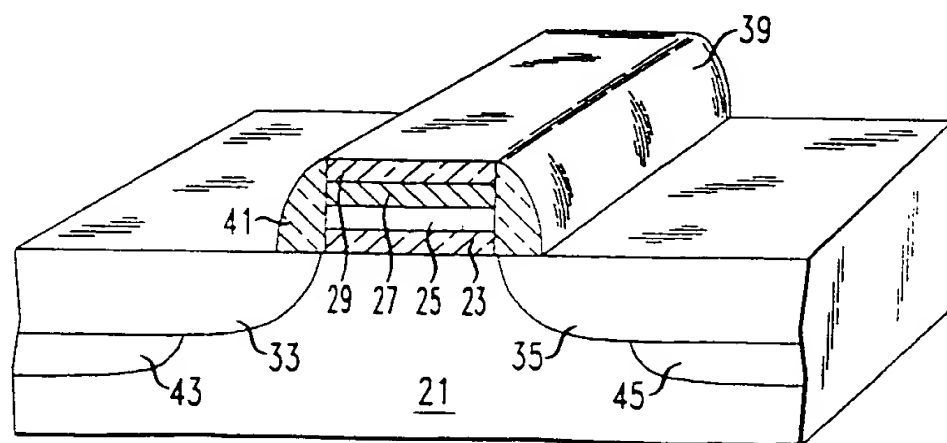
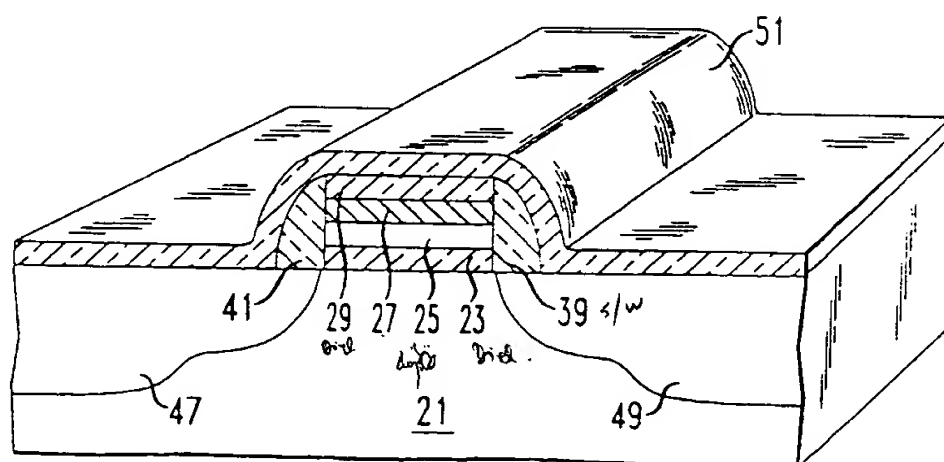


FIG. 5



TEOS are deposited. The PETEOS layer may be patterned using a gate mask. The patterned PETEOS may be utilized as a hard mask to pattern the titanium nitride polysilicon and oxide layers thereby producing the structure of FIG. 2. It will be noted that titanium nitride layer 27 is now covered by protective PETEOS layer 29 and that the plasma process utilized to form PETEOS layer 29 has not caused any appreciable oxidation of titanium nitride shunt layer 27.

Turning to FIG. 3, LDD (lightly doped drain) source and drain implants 33 and 35 are performed. Next, a blanket layer of PETEOS or silicon nitride or TEOS denoted by reference numeral 37 is formed. Next, an (optional) implant thermal activation of the LDD implant step may be performed.

Next turning to FIG. 4, blanket layer 37 is isotropically etched to produce spacers 39 and 41. Implants 43 and 45 designed to complete the source-drain regions may also be performed. It will be thus noted that the titanium nitride layer 27 is effectively encapsulated and protected by layer 29 and spacers 39 and 41.

Turning to FIG. 5, lightly-doped drain structures formed by implantations 33 and 43 have been designated by a single reference numeral 47. Similarly, lightly-doped drain structure designated by reference numerals 35 and 45 have been designated by a separate reference numeral 49. Next, a blanket dielectric layer 51 which may be a bilayer of, for example, TEOS beneath a material chosen from the group of BPTEOS or LPCVD TEOS or PETEOS, is formed. After dielectric 51 has been formed, it is smoothed by flowing it at a temperature of between 800°C and 900°C. The thermal smoothing of dielectric 51 also simultaneously accomplishes an annealing of source/drain regions 47 and 49. The thermal smoothing step is performed in an atmosphere with no more than 2% oxygen. Because of the minimal quantity of oxygen present, temperatures as high as 900°C may be used without risk of damage to layer 27. (Of course, in embodiments which do not utilize layer 27, there is not such a severe restriction on the oxygen atmosphere.) Thus, the same thermal processing step at this point of the process simultaneously smooths dielectric 51 while accomplishing a source/drain activation at the same time. Thus, thermal budget is reduced. Furthermore, the thermal heating step at this point of the process also prevents out-diffusion of boron dopant from those portions of substrates 21 which are doped with boron because no source/drain contact windows have been opened. (If source/drain contact windows had been opened, a thermal processing step would induce some boron present in substrate 21 to out-diffuse.)

From this point, further processing may continue such as the opening of windows for source and drain regions, filling of the windows with conductive material, deposition of further interlayer dielectrics and conductors, etc.

## Claims

### 1. An integrated circuit comprising

a substrate (11);  
a gate structure comprising a patterned dielectric layer (23), said dielectric layer having first and second portions over said substrate;  
a layer of patterned n doped polysilicon (25) over a first portion of said patterned dielectric layer;  
a layer of patterned p doped polysilicon (31) over said patterned dielectric layer (23) and adjacent said layer of patterned n doped polysilicon (25);  
a patterned layer of conductive material (27) over said n doped polysilicon (27) and over said p doped polysilicon (31);  
a patterned dielectric layer (29) over said layer of conductive material (27); said dielectric layer (29) not contacting said substrate;  
said gate structure also having sides and having spacers (41, 39) contacting said sides, whereby said conductive layer is enclosed by (a) said patterned dielectric layer (29), (b) said spacers (41, 39), (c) said n doped polysilicon (25), and (d) said p doped polysilicon (31).

2. The device of claim 1 in which said conductive material (27) is titanium nitride.
3. The device of claim 1 in which said patterned dielectric (29) is made from a material selected from the group consisting of plasma enhanced TEOS, SOG and LTO.
4. The device of claim 1 in which said spacers (41, 39) made from a material chosen from the group consisting of PETEOS, silicon nitride, and TEOS.
5. A method of integrated circuit fabrication comprising

forming adjacent n (25) and p doped gates (31) over a substrate;  
forming a conductive shunt layer (27) over said gates, said conductive shunt layer having a top and sides;  
forming a patterned dielectric layer (29) covering the top of said conductive shunt layer (27) and not covering said substrate;  
forming spacers (41, 39) which contact said sides of said conductive shunt layer.

6. The method of claim 5 in which said conductive shunt (27) is formed from silicon nitride.
7. The method of claim 5 in which said patterned die-

lectric (29) is formed from a material chosen from the group consisting of PETEOS, SOG and LTO

8. The method of claim 5 in which said spacers (41, 39) are formed from a material chosen from the group consisting of PETEOS, silicon nitride and TEOS

9. The method of claim 5 further including the steps of:

forming source and drain regions (47, 49) by embedding dopants in said substrate;

forming a blanket dielectric (51) overlying said source (47, 49) and drain regions

performing a thermal heating step to thereby simultaneously activating said dopants and smoothing said dielectric (51);

opening windows in said dielectric, thereby exposing said source and drain regions (47, 49)

10. A method of integrated circuit fabrication comprising:

forming an oxide layer upon a substrate (23)

forming a polysilicon layer upon said oxide layer;

doping a first portion of said polysilicon layer with n-type dopant (25);

doping a second portion of said polysilicon layer with p-type dopant (31)

forming a layer of titanium nitride (27) upon said polysilicon layer;

forming a layer of first dielectric material (29) upon said polysilicon layer;

patterning said first dielectric layer (29) by at least partially etching said first dielectric layer (29) in the presence of a patterned resist

patterning said titanium nitride layer (27), and said polysilicon layer (25) and said oxide layer (23) using said patterned first dielectric layer as

a mask (29); thereby exposing a portion of said substrate and forming an n doped gate (25) adjacent a p doped gate (31); said gates being

shunted by a patterned titanium nitride layer (27)

forming a blanket layer of a second dielectric material over said gates and over said exposed portion of said substrate

isotropically etching said blanket layer to form spacers (41, 39) adjacent said n doped gate (25) and said p doped gate (31)

11. The method of claim 10 further including the steps of:

forming source and drain regions (47, 49) by embedding dopants in said source and drain regions

forming a blanket layer of undoped oxide (51) over said gate and said source and drain regions

forming a blanket layer of doped oxide over said layer of undoped oxide

performing a thermal heating step at a temperature between 800°C and 900°C to thereby simultaneously activate said dopants and smooth said doped dielectric

opening windows through both said dielectrics thereby exposing said source and drain regions

12. A method of integrated circuit fabrication comprising:

forming source and drain regions in a substrate (47, 49), by implanting dopants into said substrate;

forming a dielectric (51) overlying said source and drain regions;

performing a thermal heating step which simultaneously activates said dopants and smooths said dielectric by causing said dielectric to flow

opening a window through said dielectric thereby exposing a said source or drain region

13. The method of claim 12 in which said dielectric (51) is made from a material chosen from the group consisting of BPTEOS, LPCVD-TEOS or PETEOS

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